

Specification:

Please amend paragraph 0013 in the specification with paragraph 0013 listed below. No new matter has been added.

[0013] The present invention may be implemented by hardware, software, firmware, microcode, or any combination thereof. When implemented in software, firmware, or microcode, the elements of the present invention are the program code or code segments to perform the necessary tasks. A code segment may represent a procedure, a function, a subprogram, a program, a routine, a subroutine, a module, a software package, a class, or any combination of instructions, data structures, or program statements. A code segment may be coupled to another code segment or a hardware circuit by passing and/ or receiving information, data, arguments, parameters, or memory contents. Information, arguments, parameters, data, etc. may be passed, forwarded, or transmitted via any suitable means including memory sharing, message passing, token passing, network transmission, etc. The program or code segments may be stored in a processor readable medium ~~or transmitted by a computer data signal embodied in a carrier wave, or a signal modulated by a carrier, over a transmission medium~~. The "processor readable medium" may include any medium that can store or transfer information. Examples of the processor readable medium include an electronic circuit, a semiconductor memory device, a ROM, a flash memory, an erasable programmable ROM (EPROM), a floppy diskette, a compact disk (CD-ROM), an optical disk, a hard disk, a fiber optic medium, ~~a radio frequency (RF) link~~, etc. The computer data signal may include any signal that

can propagate over a transmission medium such as electronic network channels, optical fibers, ~~air~~, electromagnetic, ~~RF-links~~, etc. The code segments may be downloaded via computer networks such as the Internet, Intranet, etc.

Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend claims 1 and 29.

1. (Currently Amended) A method comprising:

if throttling is enabled,

enabling a system management interrupt (SMI) timer;

determining a processor state of a processor upon expiration of the **SMI** ~~a system management interrupt (SMI)~~ timer, the processor state being one of an operational state and a low power state;

loading the SMI timer with a timer value based on the processor state, the timer value being one of a first value and a second value; and

transitioning the processor to one of the operational state and the low power state according to the processor state.